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SEU Test Techniques for 256k Static RAMs and Comparisons of Upsets Induced by Heavy Ions and Protons

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Test procedures needed to observe the single event phenomena of various 256k CMOS/NMOS static
RAMs are described. The tests were conducted with both protons and heavy ions, yielding cor-
related comparisons of results. We obtained most of the single event vulnerability data
using EDI EDH8832C, IDT IDT71256, OMNI-WAVE OW62256, and RCA XCDM62256 32k x 8 static RAMs.
Among the four device types only OW62256s were resistant to single event latch-up (SEL).
Estimates of the single event upset (SEU) rate in space show that OW62256s are the least sus-
ceptible devices. Also, our test and data reduction methods have taken into consideration
multiple upsets caused by a single ion, the effect of read/write access time, and scaling
related to feature size. The scaling study was made possible by comparing the SEU test
results of an additional four types of radiation hardened IDT static RAMs: IDT6116V
(2k x 8), IDT6167 (16k x 1), IDT7164 (8k x 8), and IDT7187 (64k x1).

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1. Introduction

The memory cell density of a RAM has been increasing in recent years. It is therefore inevitable that the techniques used in evaluating the single event upset (SEU) susceptibilities of high density RAMs have become more complex. We have chosen four types of 256k static RAMs as test samples of high density RAMs in order to investigate the various aspects of the SEU phenomena. Whenever it is needed, we have incorporated new test procedures and equipment especially to accommodate a large number of cells in a die. The devices are non-radhard EDI EDH8832C (Mitsubishi die), IDT IDT71256 (IDT die), OMNI-WAVE OW62256 (Hitachi die), and RCA XCDM62256 (Seiko die). All devices are organized as 32k x 8, have feature sizes of about 1.25 microns, and incorporate the NMOS memory cells surrounded by CMOS/bulk peripheral/control circuits. The four-transistor NMOS cell is shown in Figure 1. The resistor value is expected to be in the tens of gigaohms at room temperature. Having four device types of very similar organization, we can compare the results of the various tests in a more meaningful manner.
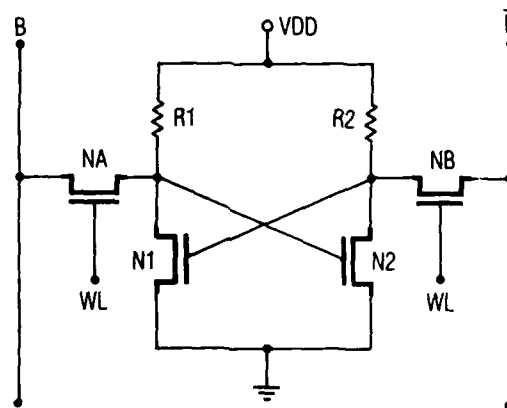
Figure 1. Static RAM Cell with High Resistance Loads.

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2. Test Techniques

Figure 2 is a schematic representation of the test apparatus which consists of (a) the beam delivery hardware and (b) the device tester. New features have been added to the standard SEU test procedure. Briefly, the basic procedure used to measure the SEU susceptibility of a RAM is as outlined below:[1]

An individual chip is irradiated with a known total fluence of particles and the total number of errors is recorded. The bit error probability or cross–section (σ) is calculated from the expression

$$\sigma = (N/F) \sec \theta$$

where N and F are the number of bit errors and beam fluence, respectively, and θ is the incident angle of the beam measured with respect to the chip–surface normal.

Figure 2. Schematic Presentation of the Test Set-up.
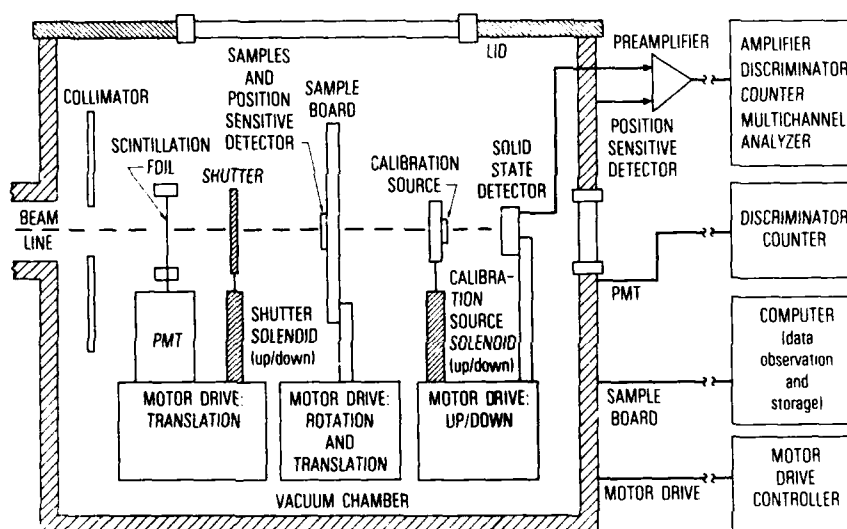
The device power supply current is closely monitored to check for occurrence of latch–up. During latch–up, more than one current path may open up and consequently the device under test will draw increased amounts of current, which can vary from event to event.

We used beams of H (50 MeV), O (430 MeV), N (68 MeV), Ne (90 MeV), Ar (180 MeV), Cu (290 MeV), and Kr (360 MeV).

The first technical factor to be considered is the read/write time. Several years ago this question could not be pursued, because we exposed the device to the ion beam after the device was written and then interrogated for errors (read) only after the shutter to the beam had been closed. This totally static technique is now augmented by more dynamic testing in which RAMs are continuously interrogated, errors detected/corrected and documented while the device under test is exposed to the beam. With this procedure, we can vary the read/write access time from the minimum value imposed by the device specification to a large number. Dependence of SEU results on the read/write cycle time is shown below. It should be noted that the operation of a RAM in space varies from very static to very dynamic, depending upon the application.

For several years, we have been recording the number of upsets (N) in terms of the address of the word in which the error occurred, the "polarity" of the upset (i.e., from zero to one or from one to zero) and the location of the upset bit in the word. All data are stored in the order of occurrence in our test computer as an error table for archival use. Given the error table and the manufacturer's "bit map", we can address the question of multiple bit errors caused by one ion. This is our second technical consideration. A "bit map" correlates the actual physical location of the bits on the die with their external address as determined by the voltage levels on the device address pins, and is essential in determining error multiplicity associated with individual particle hits.

We need to measure the multiplicity in order to provide a guide in selecting the type of EDAC (error detection and correction) feature of the system incorporating the devices under test. The process of data analysis should take into account the dependence of error multiplicity on the relevant properties of the beam (e.g., LET and particle range) and of the test device, such as geometry and fabrication process.

The soft error and latch-up susceptibilities are expected to vary in different thermal environments. We have used a heater just below the device under test to attain higher temperature environments.[2] Temperature is another factor that we should take into consideration.

The question concerning the Single Event Disturbed (SED) phenomenon may apply to these static RAMs, which incorporate four-transistor NMOS cells.[2]

3. Test Results and Comments

   Plots of SEU cross–section vs. linear energy transfer (LET) curves for the four device types are shown in Figures 3 through 6. In these curves, the cross–section values have not been corrected for error multiplicity, and hence represent a gross measure of device suscep- tibilities. It is important to note that the threshold LET values of EDI, IDT, and RCA de- vices are very similar to each other and that they differ from that of the OMNI–WAVE de- vices. These results were taken at room temperature The read/write access time was about 300 nanoseconds (see below for comparisons of the access time). The die sizes for EDH8832C, IDT71256, OW62256, XCDM62256 are 0.36 cm², 0.34 cm², 0.34 cm², and 0.36 cm², respectively. So, the saturation cross–sections are roughly comparable to the die sizes. The latch–up data obtained from the EDI, IDT, and RCA devices are shown in Figures 7 through 9, respectively. The OMNI–WAVE devices showed no sign of latch–up even at the LET of 120 MeV/(mg/cm²). The saturation latch–up cross–section for IDT devices is 7×10^{-5} cm²/device, whereas for the EDI and RCA devices the cross–sections are some- where between 1×10^{-3} and 3×10^{-3} cm²/device.

Figure 3. SEU Test Results for EDH8832C (32k x 8) RAMs.

Figure 4. SEU Test Results for IDT71256 (32k x 8) RAMs.

Figure 5. SEU Test Results for OW62256 (32k x 8) RAMs.

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Figure 6. SEU Test Results for XCDM62256 (32k x 8) RAMs.

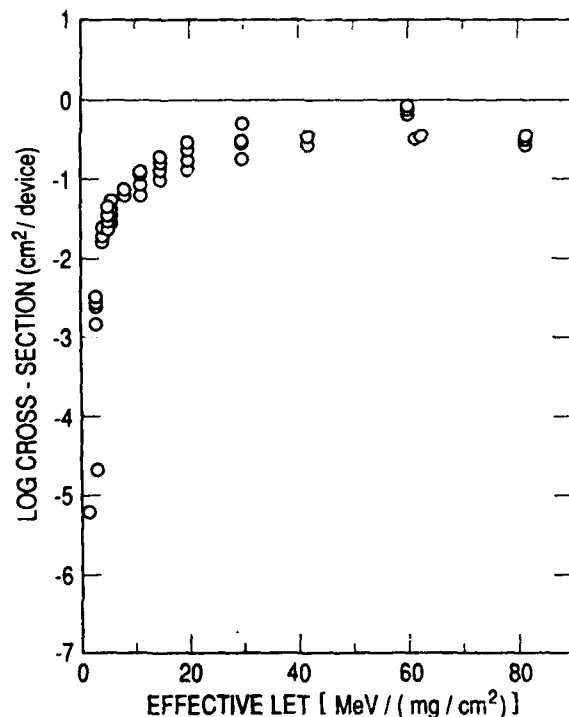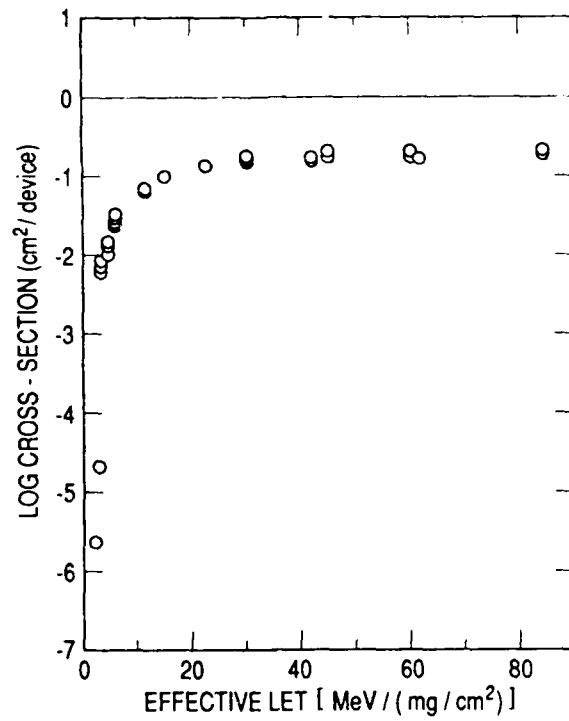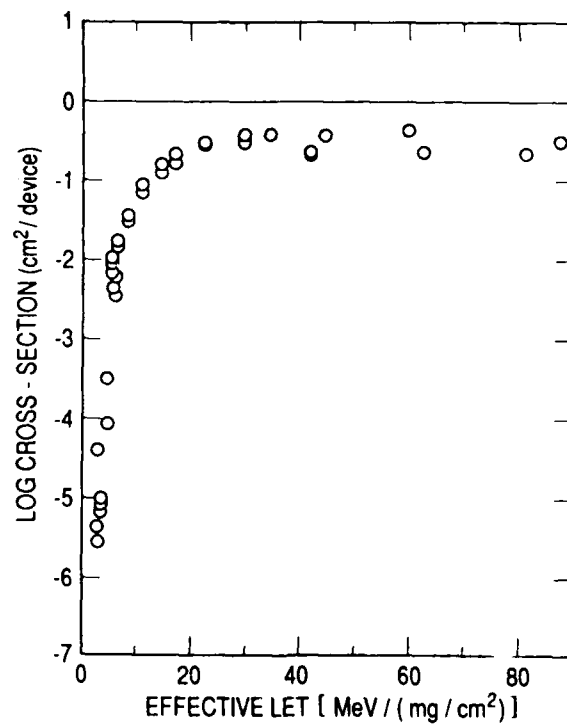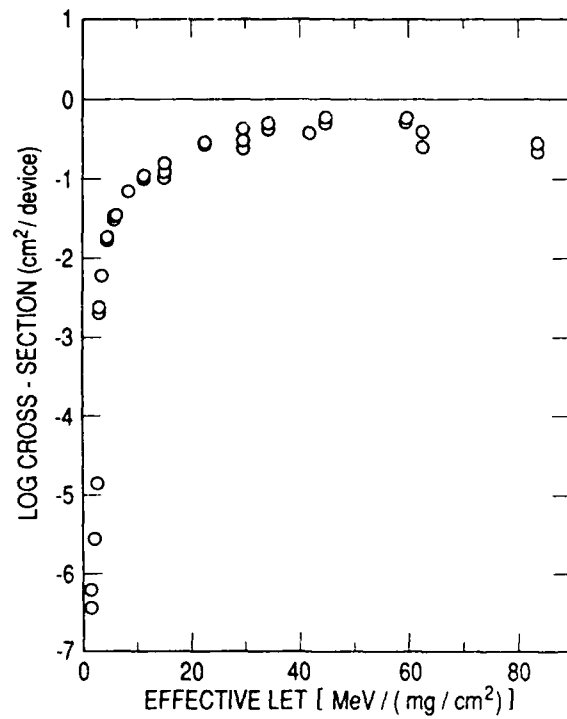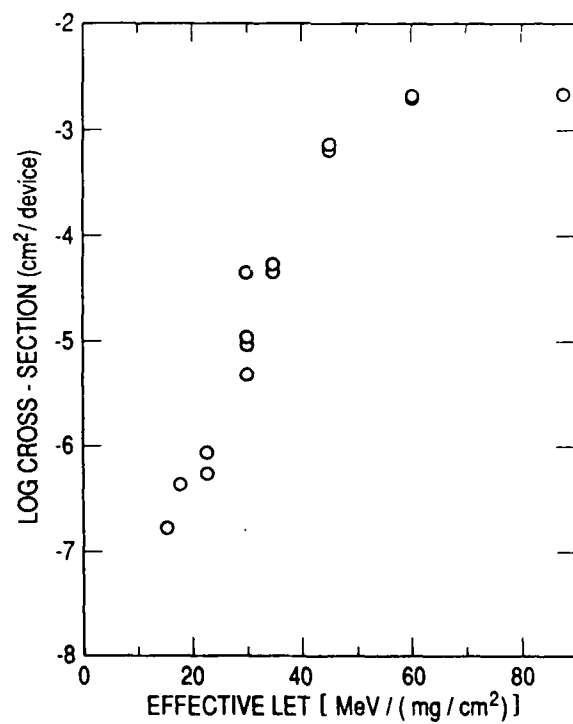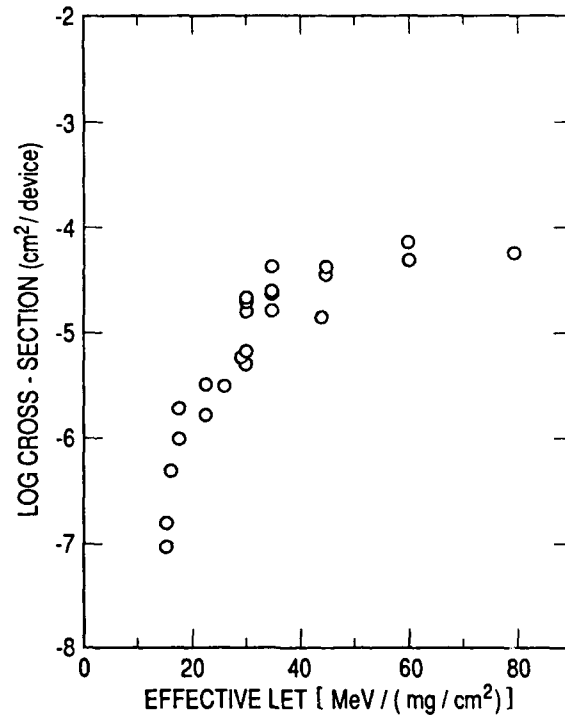Figure 7. Latch-up Test Results for EDH8832C (32k x 8) RAMs.

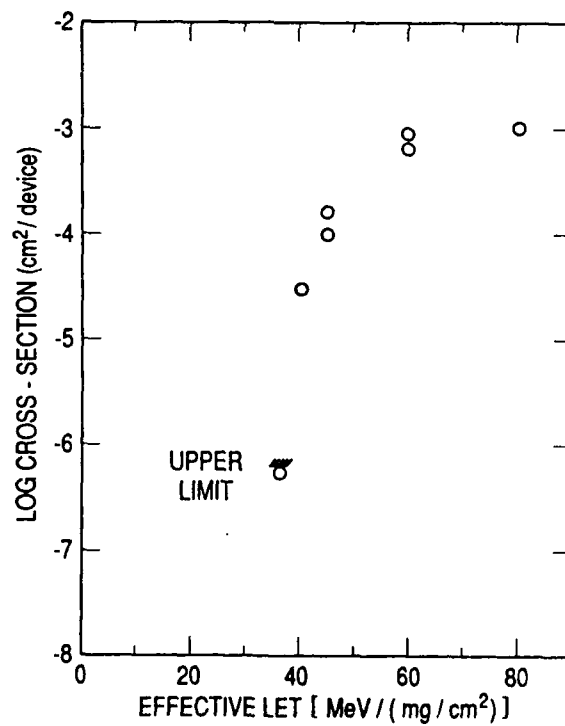Figure 8. Latch–up Test Results for IDT71256 (32k x 8) RAMs.

Figure 9. Latch–up Test Results for XCDM62256 (32k x 8) RAMs.

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The supply current was monitored during the latch-up tests. We observed the following holding current values:

EDH8832C: The holding current was less than 300 mA, but above 200 mA. There were one or two modes of parasitic SCR current paths with different holding current values:

IDT71256: The holding current was less than 300 mA, but above 50 mA. Most of the time it was about 80 mA. There were several modes of the SCR paths with different holding current values.

RCA62256: The holding current was less than 300 mA, but above 150 mA. There were one or two modes of the SCR paths with different holding current values.

It took about 0.2 ms for the supply voltage to drop to a small value upon onset of the latch-up condition. The effect was monitored at the power supply located in the control room, a considerable distance from the test chamber. We believe the major contributing factor of the long time interval was high capacitance of the power supply. The RC time constant is about 0.3 ms, if R = 10 ohms and C = 30 uF.

Some latch-up and soft error upset tests at 60° were also performed, and we found no deviations from the room temperature results. We plan to extend the temperature range to 125°C in the near future.

The read/write access time was varied from about 130 nanoseconds to a large value to observe its effect on the upset rate. This test was conducted at several LET values. The test results obtained with Ne ions, which do not cause latch-up in any of the devices, are shown in Table 1. The effect of the read/write access time is less than 10% for all except IDT devices. The IDT devices showed about 30% cross-section increase in the dynamic environment. This result differs from data we obtained in a previous study of some 16k IDT static RAMs (IDT6116 2k x 8 RAM and IDT71681 4k x 4 RAM), where we found that both the dynamic and static tests yielded the same results.[3] It is possible that SED type events in the high density IDT RAMs are a cause of the discrepancy.

Multiple bit errors can be caused by a hit of a single ion. Indeed we have found double, triple, quadruple, even quintuple bit errors, as shown in Table 2. All four device types showed multiple errors at all angles when struck by some ions. (The distribution of charge deposited by an ion extends over an area larger than that of a single cell for these devices, and multiple errors result.) This effect raises the question about the meaning of the gross cross-section, calculated in the usual way. Clearly, such a cross-section does not correlate with the geometrical size of the "sensitive area." We need to correct the gross cross-section in order to determine the sensitive area of the die. According to the bit map, all devices are organized in such a way that none of the bits in a single byte address is located in close physical proximity to another bit from the same byte. It is not surprising, therefore, that we did not oberve any multiple errors in any single word. By precluding multiple errors in a single word, the above layout of memory cells makes possible the application of EDAC schemes. The strategy fails only when an ion penetrates along the surface of a device. However, the solid angle for these events is quite low.

Table 1. SEU Cross-section vs Read/Write Access Time. (90 MeV Ne ions were used for this test. The angle between the beam and the chip-surface normal was 0 degrees.)

Device Type	Read/Write Access Time (ns)	Cross-section (cm²/device)
EDH8832C	130	3.0 E-2
	650	2.8 E-2
	2000	2.5 E-2
	Static	2.7 E-2
IDT71256	130	2.5 E-2
	650	2.5 E-2
	2000	2.3 E-2
	Static	1.7 E-2
OW62256	130	.80 E-2
	650	.76 E-2
	2000	.78 E-2
	Static	.78 E-2
XCDM62256	130	3.0 E-2
	650	3.1 E-2
	2000	2.9 E-2
	Static	3.0 E-2

Table 2. Multiple Errors

ION:	O			N			Ne			Ar			Cu			Kr			
ANGLE: (deg)	0	48	60	0	48	60	0	48	60	0	48	60	0	48	60	0	48	60	
EDH8832C (%)	100	100	100	100	100	100	100	100	100	100	94	77	81	53	55	62	56	48	SINGLE
											6	18	19	38	39	29	31	52	DOUBLE
												5		9	6	9	13		TRIPLE
																			QUADRUPLE
																			QUINTUPLE
IDT71256 (%)	100	98	91	100	100	98	96		89	85	68	74	78	75	56	81	67	72	SINGLE
		2	9			2	4		11	13	32	21	20	25	41	19	28	28	DOUBLE
										2		5	2		3		5		TRIPLE
																			QUADRUPLE
																			QUINTUPLE
OW62256 (%)				100	100	100	100	100	100	94	78	83	64	56	44	71	78	52	SINGLE
										6	20	12	33	26	33	26	22	39	DOUBLE
											2	5	3	15	15	3		6	TRIPLE
															8			3	QUADRUPLE
														3					QUINTUPLE
XCDM62256 (%)	100	100	100	100	100	100	100	100	100	100	94	70	59	48		64	62	64	SINGLE
											6	24	35	42		33	29	33	DOUBLE
												6	6	10		3	9	3	TRIPLE
																			QUADRUPLE
																			QUINTUPLE

The 50 MeV proton data were taken within several days of the heavy ion tests. The proton upset cross-sections were measured at three orientations of the device with respect to the beam, as shown in Table 3. The orientation can be characterized by the angle between the beam incident line and the chip–surface normal line. It is important to note that the cross-sections for OW62256 were substantially lower than the rest — the same result we saw with heavy ions.

Table 3.   Proton SEU Cross–section vs Incident
            Angle with the Chip–surface Normal
            (50 MeV protons were used)

Device Type	Incident Angle (degrees)	Cross–section (cm²/device)
EDH8832C	0	2.0 E-7
	48	2.7 E-7
	60	4.8 E-7
IDT71256	0	1.3 E-7
	48	1.7 E-7
	60	2.5 E-7
OW62256	0	4.6 E-8
	48	7.2 E-8
	60	8.7 E-8
XCDM62256	0	2.3 E-7
	48	3.3 E-7
	60	3.8 E-7

Total dose testing, conducted separately from the SEU tests with a ^{60}Co gamma source at the NASA Goddard Space Flight Center, indicated that the total dose tolerances of RCA, EDI, IDT, and OMNI-WAVE devices are 2-4, 4-6, 6-8, and 6-10 kRad (Si), respectively. The OMNI-WAVE devices again showed a high tolerance suggesting that there may be a single factor which makes the OMNI-WAVE devices more tolerant against total dose and single event phenomena caused by protons and high Z particles.

In the following section, we would like to compare the upset rate of several static RAMs of varying feature size. Therefore, we will describe the SEU/SEL test results of lower density (than that of a 256k device) static RAMs that we happened to have in our archive of test data. The most convenient ones are radiation–hardened NMOS/CMOS devices manufactured by IDT. Radiation–hardened devices are normally designed for a higher total dose environment with a high resistance to latch–up. However, the cell sizes of both radiation–hardened and non–hardened RAMs are essentially the same for IDT devices of the same memory organization, and therefore, we can use the test data of the radiation–

hardened IDT devices along with the non–hardened IDT 256k static RAMs for the scaling study (see the following section for the details of this study). The radiation-hardened static RAM types are: IDT6116V (2k x 8), IDT6167X (16k x 1), IDT7164 (8k x 8), and IDT7187 (64k x 1). The soft error cross–section curves for each device type are reproduced as shown in Figures 10 through 13. The results also showed that the devices are resistant to single event latch–up. It is expected that these devices can tolerate about 30 kRad (Si) of total dose.
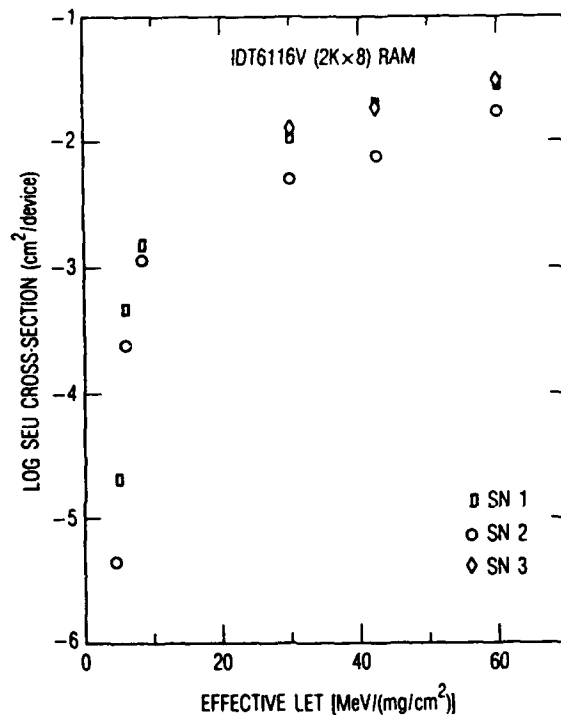

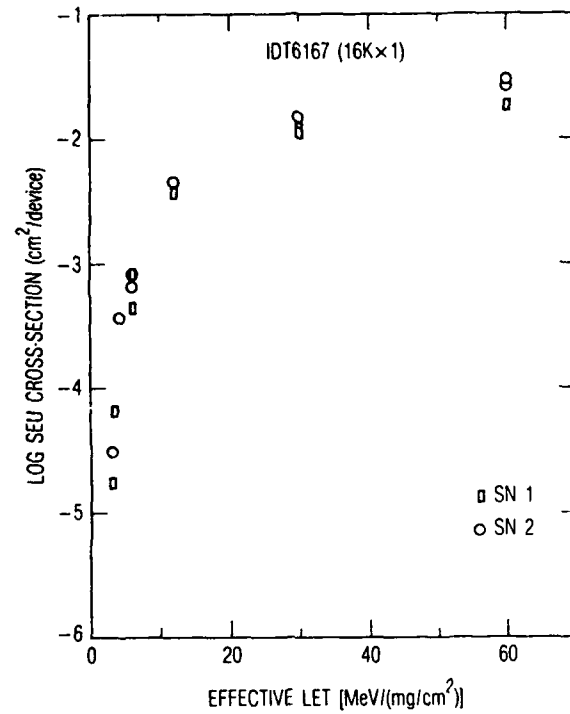Figure 10. SEU Test Results for IDT6116V (2k x 8) RAMs.

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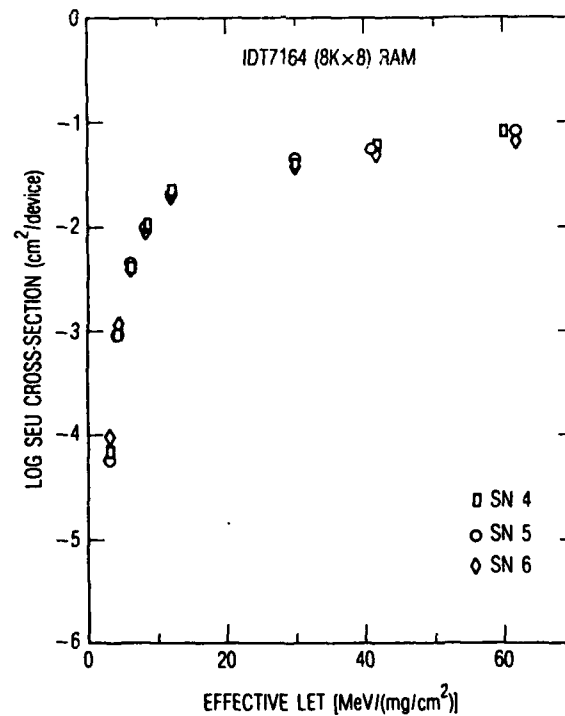Figure 11. SEU Test Results for IDT6167X (16k x 1) RAMs.

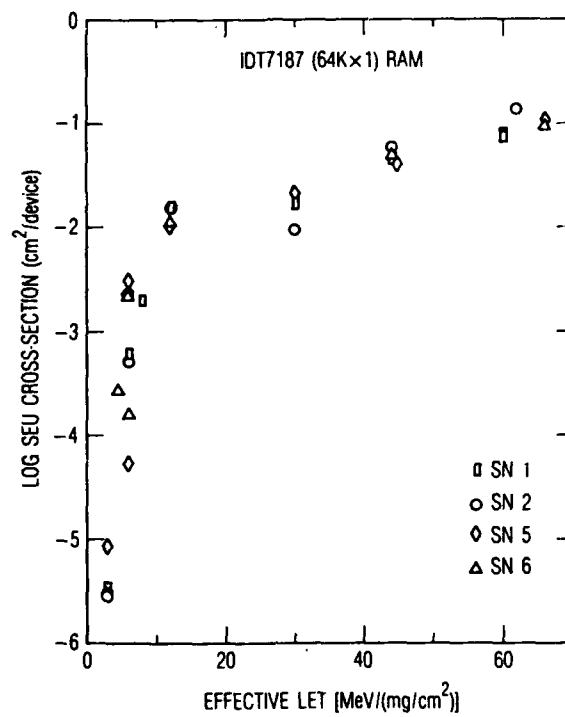Figure 12. SEU Test Results for IDT7164 (8k x 8) RAMs.

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Figure 13. SEU Test Results for IDT7187 (64k x 1) RAMs.

4. Discussion and Conclusions

The high current condition during latch-up can be cleared by installing a monitoring circuit that turns the power off and back on again. The latch-up current monitor should respond to latch-up within several microseconds, while taking into account the fact that the rise time in the value of the measured current depends on the RAM-board capacitance and may extend into the millisecond range. Furthermore, power should remain off until the charge remaining on the circuit capacitors is insufficient to sustain the latch-up condition.

The existence of multiple errors caused by one ion makes the task of estimating the SEU rate difficult. However, we can obtain an upper limit of the upset rate by pretending a lack of knowledge about multiple errors and assuming each observed error to be a hit in the sensitive parallelepiped region used by the Adams' code (see Appendix). The results of upset estimates for the four device types are as follows:

SEU rate in space(upset/bit-day)

(Cosmic-rays during the solar min + "90% worst case" flares)

	EDH8832C	IDT71256	QW62256	XCDM62256
Geosynchronous Orbit:	1.0 E-4	5.3 E-5	3.1 E-5	8.2 E-5

A model is needed for more accurate prediction of upset rates: a model accounting for the multiple bit errors which we have shown to take place in static VLSI RAMs. The effect of read/write access time on SEU rate and the SED phenomenon may be ignored when estimating the upset rate in the present context.

Even though it is essential to characterize these devices for the full range of temperatures, we simply had not had a chance to conduct the SEU/SEL testing of these devices at temperatures beyond 60°C. The effect of the temperature ranging from room temperature to 60°C in these devices, however, is not great (less than a few percent). In general, there are only small amounts of data available for the high temperature testing of the four-transistor NMOS static RAMS. Our past experience with IDT6116 indicates that the dependence of the SEU susceptibility on the temperature exists only at higher temperatures (around 100°C).[2] A major incentive to conduct the test will emerge when we can get the temperature coefficient of the resistor loads.

The testing of these high density 256k RAMs can yield additional information with which one can make progress in some studies such as the verification of the scaling values and other phenomenological studies.[5] For instance, we can address the issue of SEU sensitivity as a function of scaling to smaller and smaller devices by producing a comparison of upset rates of several IDT static RAMs ranging from 16k to 256k, as shown in Table 4. This table is "complete" with the 256k data.

Table 4. A Comparison of the Upset Rates of IDT Static RAMs at the Geosynchronous Orbit for Two Values of the Threshold LETs (Galactic cosmic-rays only during the solar minimum)

Device Type	Saturation Cross-section	Threshold LET $(MeV/(mg/cm^2))$	Upset Rate in Space (Errors/bit-day)
6116V (2k x 8)	159 μ^2/bit	6 — 10	1.3 E-5 — 4.3 E-6
6167X (16k x 1)	165	5 — 10	1.8 E-5 — 4.5 E-6
7164 (8k x 8)	125	4 — 7	2.1 E-5 — 7.0 E-6
7187 (64k x 1)	153	5 — 7	1.7 E-5 — 8.8 E-6
71256 (32k x 8)	80	4 — 6	1.3 E-5 — 5.9 E-6

Finally, it will be meaningful to investigate in more detail the OMNI-WAVE device from the design and fabrication points of view, since the OW62256 clearly stands out as being the superior one of the four device types, as far as hardness against radiation effects in space is concerned. To date, however, we know only that the CMOS section of the die does not have an epitaxial layer, and that a special lay-out technique has contributed to the apparent resistance to latch-up.[6]

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Appendix: Upset Rate Estimation

Estimates of upset rate in space were made using the cyclotron data and the Cosmic Ray Upset Model (CRUM) code developed by J. Adams at the Naval Research Laboratory.[4] This code assumes that the volume sensitive to upset is a rectangular parallelepiped, and that a definite critical charge for upset is associated with the memory-cell circuit. Given the volume, dimensions, critical charge, orbital parameters and amount of shielding, the program computes the number of particles per day which, in traversing the sensitive volume, generate an amount of charge in excess of the critical charge for upset. This number, multiplied by the total number of sensitive elements on the chip, constitutes the upset rate of the device.

Due to lack of information concerning device geometry, process and circuit design, certain assumptions were made about these parameters, which probably are at variance with their actual values. However, these assumptions lead to conservative estimates of upset rate, in the sense that the actual rate may be up to an order of magnitude lower than the predicted one. The assumptions which were made are as follows:

1. The sensitive volume for each memory cell is a square slab one micron thick, with an area equal to the maximum cross-section divided by the number of bits on the device.

2. The critical charge for upset is the threshold LET times the slab thickness (one micron). The threshold LET is the value of LET at which the cross-section is 1% of the saturated cross-section (unless otherwise stated).

3. The device is surrounded by 0.125-inch-thick shielding material (Al).

LABORATORY OPERATIONS

The Aerospace Corporation functions as an "architect-engineer" for national security projects, specializing in advanced military space systems. Providing research support, the corporation's Laboratory Operations conducts experimental and theoretical investigations that focus on the application of scientific and technical advances to such systems. Vital to the success of these investigations is the technical staff's wide-ranging expertise and its ability to stay current with new developments. This expertise is enhanced by a research program aimed at dealing with the many problems associated with rapidly evolving space systems. Contributing their capabilities to the research effort are these individual laboratories:

Aerophysics Laboratory: Launch vehicle and reentry fluid mechanics, heat transfer and flight dynamics; chemical and electric propulsion, propellant chemistry, chemical dynamics, environmental chemistry, trace detection; spacecraft structural mechanics, contamination, thermal and structural control; high temperature thermomechanics, gas kinetics and radiation; cw and pulsed chemical and excimer laser development including chemical kinetics, spectroscopy, optical resonators, beam control, atmospheric propagation, laser effects and countermeasures.

Chemistry and Physics Laboratory: Atmospheric chemical reactions, atmospheric optics, light scattering, state-specific chemical reactions and radiative signatures of missile plumes, sensor out-of-field-of-view rejection, applied laser spectroscopy, laser chemistry, laser optoelectronics, solar cell physics, battery electrochemistry, space vacuum and radiation effects on materials, lubrication and surface phenomena, thermionic emission, photo-sensitive materials and detectors, atomic frequency standards, and environmental chemistry.

Computer Science Laboratory: Program verification, program translation, performance-sensitive system design, distributed architectures for spaceborne computers, fault-tolerant computer systems, artificial intelligence, micro-electronics applications, communication protocols, and computer security.

Electronics Research Laboratory: Microelectronics, solid-state device physics, compound semiconductors, radiation hardening; electro-optics, quantum electronics, solid-state lasers, optical propagation and communications; microwave semiconductor devices, microwave/millimeter wave measurements, diagnostics and radiometry, microwave/millimeter wave thermionic devices; atomic time and frequency standards; antennas, rf systems, electromagnetic propagation phenomena, space communication systems.

Materials Sciences Laboratory: Development of new materials: metals, alloys, ceramics, polymers and their composites, and new forms of carbon; non-destructive evaluation, component failure analysis and reliability; fracture mechanics and stress corrosion; analysis and evaluation of materials at cryogenic and elevated temperatures as well as in space and enemy-induced environments.

Space Sciences Laboratory: Magnetospheric, auroral and cosmic ray physics, wave-particle interactions, magnetospheric plasma waves; atmospheric and ionospheric physics, density and composition of the upper atmosphere, remote sensing using atmospheric radiation; solar physics, infrared astronomy, infrared signature analysis; effects of solar activity, magnetic storms and nuclear explosions on the earth's atmosphere, ionosphere and magnetosphere; effects of electromagnetic and particulate radiations on space systems; space instrumentation.

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